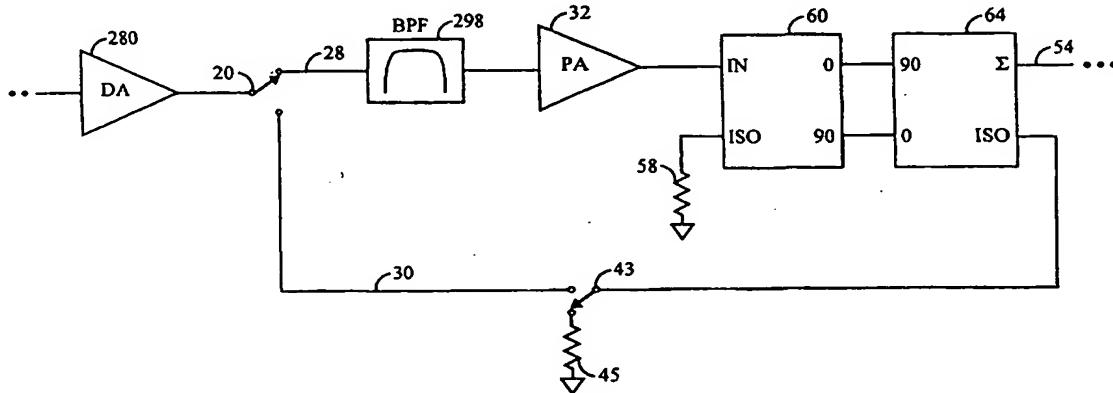




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(54) Title: HIGH EFFICIENCY SWITCHED GAIN POWER AMPLIFIER



(57) Abstract

A power amplifier circuit arrangement including a driver amplifier, a switch, an amplifier path having a band pass filter and a power amplifier, and a bypass path which bypasses the power amplifier when excess gain and output power are not needed. When an RF-analog signal from the driver amplifier is switched to the amplifier path, the signal is band-pass filtered and amplified. Then the signal is split into an in-phase and a quadrature signal. Either the in-phase or the quadrature signal is inverted and summed with the other of the in-phase or quadrature signal, and the summed signal is transmitted to an output port. When the RF-signal from the driver amplifier is switched to the bypass path, the power amplifier is turned off and the bypass path directs the signal to the output of the power amplifier, which appears as a high impedance to the signal. The signal reflects off the power amplifier to the output port.

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HIGH EFFICIENCY SWITCHED GAIN POWER AMPLIFIER

BACKGROUND INFORMATION

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I. Field of the Invention

The present invention relates generally to power gain control for a power amplifier circuit and particularly to a power application circuit having greater power conservation in wireless communication device, such as a CDMA wireless phone.

2. Description of the Related Art

In many electronic environments, such as most hand-held communication systems including code-division-multiple-access (CDMA) or any form of time-division-multiple access (TDMA) technology, RF power output from a mobile unit varies in large dynamic ranges. In a CDMA radiotelephone system, multiple signals are transmitted simultaneously at the same frequency. The signals are spread with different digital codes, thus allowing detection of the desired signal while the unintended signals appear as noise or interference to the receiver. Spread spectrum systems can tolerate some interference, and the interference added by each new mobile station increases the overall interference in each cell site. Each mobile station introduces a unique level of interference, which depends on its received power level at the cell site.

The CDMA system uses power control to minimize mutual interference. A precise power control is critical to avoid excessive transmitter signal power that is responsible for contributing to the overall interference of the system. Power of the individual mobile stations varies with the distance between the mobile station and the base

station and the number of other subscriber mobile stations in that base station or sector.

In a typical hand-held wireless unit, the power amplifier is biased class AB to reduce power consumption during periods of low transmit power, but power continues to be consumed. Typically an isolator is used to isolate the power amplifier from the effects of load impedance in subsequent stages. One method to avoid continuous battery draw is to employ a means to bypass the amplifier with switches, and then remove DC power from the amplifier. Such a power amplifier circuit has a power amplifier and an isolator. An RF-input is connected to a pole of a first switch. When the amplifier is on, the switch connects the RF-input to an input of the power amplifier. The RF-signal is amplified and output to the isolator, and then transmitted through the second switch to the RF-output of the power amplifier circuit. To bypass the power amplifier, the first switch connects the RF-input to the bypass path and the second switch transmits the signal to the RF-output. The switching employed introduces loss as the signal is processed. The drawback of this design is that the amplifier must overcome the added switching loss during times that higher transmit power is required. This can tend to cancel the benefits of bypassing.

SUMMARY OF THE INVENTION

What is needed in the art is a cellular phone or mobile station having power amplifier circuit which conserves power by turning off and bypassing the power amplifier when power demand is low and by using a driver amplifier ("DA") as the power output amplifier.

An object of the present invention is to increase the efficiency of power amplifier usage by providing a circuit to bypass the power amplifier or power amplifiers when power demand is low.

Another object of the present invention is to reduce the effects of power loss after a signal is amplified by a power amplifier.

Another object of the present invention is to provide an improved power amplifier which requires less parts and is less complex to build.

5 Yet another object of the present invention is to provide an improved power amplifier which is less expensive to build.

These objects and others may be realized by the invention disclosed herein. In a mobile station having a power amplifier circuit, a switch operates to direct the received signal from a driver amplifier to 10 either an amplifier path containing a band-pass filter and a power amplifier, or a bypass path. The bypass path bypasses the power amplifier when the power amplifier capability is not required. During the periods of low power operation, the amplifier is turned off. When the signal is passed through the bypass path it enters the isolated port of a hybrid 15 circuit. The signal is transmitted to the output of the power amplifier. The power amplifier appears as a large impedance which is highly reflective because it is turned off. The reflected signal is then routed to the output port or front end of the circuit. With this configuration, an output switch becomes unnecessary and the power loss after the signal is 20 amplified is reduced.

A first band-pass filter is placed in the amplification path such that filtering is also bypassed when the power amplifier is bypassed. When greater power amplification of the signal is needed, the signal flow is directed through a transmitter chain containing the first band-pass filter 25 and a power amplifier ("PA"). The first filter in the transmitter chain cleans up noise added by the DA. The PA amplifies the signal which then is transmitted through an isolator and a second filter at the output of the circuit which cleans up noise added by the PA. A benefit of bypassing the PA is that it no longer adds noise to the signal. The second 30 filter at the output of the circuit still filters the added effects of the PA, and when the signal routes through the bypass path, the second filter

reduces noise added by the driver amplifier. Therefore, the first filter becomes unnecessary when the signal is passed through the bypass path.

This power amplification circuit provides reduced loss at the end of the amplifier, whereby greater power using less current at the output 5 may be achieved. The configuration also reduces the loss in the bypass path when changing modes from amplification to bypass. The driver amplifier therefore becomes the output amplifier.

In another aspect of the present invention, bypassing the power amplifier enables the driver amplifier to be driven harder because it is the dominating source of distortion in the chain. The driver amplifier 10 may be driven to a greater degree in the non-linear region than could be accomplished when using the power amplifier. By expanding the region over which the driver amplifier is driven, the cellular phone may be operated using the driver amplifier for a longer period of time, thus 15 conserving battery power by keeping the power amplifier off for longer periods of time.

BRIEF DESCRIPTION OF THE DRAWINGS

20 The features and advantages of the present invention will become more apparent from the detailed description set forth below when taken in conjunction with the drawings in which like reference characters correspond throughout and wherein:

25 FIG. 1 is a block diagram of a mobile station of the present invention;

FIG. 2 is a plan drawing of the first embodiment of the present invention;

30 FIG. 3 provides a block diagrammatic representation of a mobile station spread spectrum transmitter in which may be incorporated an efficient power amplifier of the present invention;

FIG. 4 shows an exemplary implementation of an RF transmitter included within the spread spectrum transmitter of FIG. 2;

FIG. 5 is a plan drawing of the second embodiment of the present invention;

5 FIG. 6 is a plan drawing of the third embodiment of the present invention;

FIG. 7 is a plan drawing of the fourth embodiment of the present invention; and

10 FIG. 8 is a plan drawing of a sixth embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 illustrates a mobile station of the present invention and its 15 signal processing. A mobile station 100 comprises circuitry for interfacing with system memory and the user 102. The memory and user interface 102 is connected to a digital processor 104 which controls the signal processing. A receiving chain comprises a receiving IF/baseband signal processing circuit 106 connected to the digital processor 104, and a 20 receiving RF-signal processing circuit 108. A transmitting chain comprising a transmitting IF/baseband processing circuit 120 is connected to the digital processor 104. A transmitting RF processing circuit 122 includes the power amplifier circuit arrangement described in more detail herein.

25 A duplexer 124 controls the signal flow from the receiving chain and the transmitting chain and an antenna 126. A codec circuit 110 is connected to the digital processor 104. The circuit elements illustrated in FIG. 1, except the transmitting signal processing 122 disclosed herein, are generally known to those of ordinary skill in the art. Accordingly, the 30 foregoing description and block diagram of FIG. 1, in addition to the disclosure of the power amplifier circuit arrangement of the present

invention, sufficiently enable one of ordinary skill in the art to make and use the mobile station of the present invention.

FIG. 2 is a schematic diagram showing the power amplifier aspect of the invention. A power amplifier circuit, indicated generally by reference numeral 10, comprises a power amplifier 32, a circulator 52, a series of switches, 20, 24 and 42, and bypass paths 34 and 36 around the power amplifier 32. An RF-input 12 having an RF-signal to be amplified is connected to a pole of first switch 20. When amplification of the RF-signal is required, the power amplifier 32 is turned on and the switch 20 connects the RF-input 12, via a path 28, to an input of the power amplifier 32. The power amplifier transmits the RF-signal toward the circulator 52. The circulator 52 routes the signal to a port of the RF-output 54.

When power demand is low and the power amplifier is turned off, the switch 20 switches the RF-signal to a bypass network 48 comprising a bypass path 36 and an attenuated path 34. To send the signal through the bypass path 36, switches 24 and 42 switch to a first position such that the signal flows through bypass path 36. Switches 24 and 42 can also switch the signal to flow through the attenuated path 34. From switch 42 the signal is transmitted to an input of circulator 52. The circulator 52 routes the signal to the port connected to the output 50 of the power amplifier 32. The output of the power amplifier 50 appears as a high impedance to the signal and thus the signal is reflected back to the circulator 52, which routes the signal to the port of the RF-output 54 of amplifier circuit 10.

FIG. 3 is a schematic diagram illustrating the use of the power amplifier of the present invention in the signal processing circuitry of a mobile station. In an exemplary CDMA system, orthogonal signaling is employed to provide a suitable ratio of signal-to-noise on the mobile-station to base-station link, or the "reverse" channel. Data bits 200 consisting of, for example, voice converted to data by a vocoder, are supplied to an encoder 202 where the bits are convolutionally encoded. When the data bit rate is less than the bit processing rate of the encoder

202, code symbol repetition may be used such that the encoder 202 repeats the input data bits 200 in order to create a repetitive data stream at a bit rate which matches the operative rate of the encoder 202. In an exemplary embodiment the encoder 202 receives data bits 200 at a 5 nominal bit rate (R_b) of 11.6 kbits/second, and produced $R_b / r = 34.8$ symbols/second, where "r" denotes the code rate (e.g. 1/3) of the encoder 202. The encoded data is then provided to a block interleaver 204.

With the 64-ary orthogonal modulator 206, the symbols are grouped into characters containing $\log_2 64 = 6$ symbols at a rate of $(1/r)(R_b / \log_2 64) = 5,800$ characters/second, with there being 64 possible characters. In a preferred embodiment each character is encoded into a Walsh sequence of length 64. That is, each Walsh sequence includes 64 binary bits or "chips", there being a set of 64 Walsh codes of length 64. The 64 orthogonal codes correspond to Walsh codes from a 64 by 64 15 Hadamard matrix wherein a Walsh code is a single row or column of the matrix.

The Walsh sequence produced by the modulator 206 is provided to an exclusive-OR combiner 208, where it is then "covered" or multiplied at a combiner with a PN code specific to a particular mobile station. Such 20 a "long" PN code is generated at a rate R_c by a PN long code generator 210 in accordance with a user PN long code mask. In an exemplary embodiment the long code generator 210 operates at an exemplary chip rate, R_c , of 1.2288 Mhz so as to produce four PN chips per Walsh chip. The output of the exclusive -OR combiner 208 is split into identical 25 signals A and B. Signals A and B are input into the exclusive-OR combiners 256 and 254 of FIG. 4 as described below.

FIG. 4 is a schematic diagram showing an exemplary implementation of the RF transmitter 250 in a mobile station. In CDMA spread spectrum applications, a pair of short PN sequences, PN_1 and PN_Q , 30 are respectively provided by a PN_1 generator 252 and a PN_Q generator 254 to exclusive-OR combiners 256 and 258, along with the output A and B from exclusive-OR combiner 208 of FIG. 2. The PN_1 and PN_Q sequences

relate respectively to in-phase (I) and quadrature phase (Q) communication channels, and are generally of a length (32,768 chips) much shorter than the length of each user long PN code. The resulting I-channel code spread sequence 260 and Q-channel code spread sequence 5 262 are then passed through baseband filters 264 and 266, respectively.

Digital to Analog (D/A) converters 270 and 272 are provided for converting the digital I-channel and Q-channel information, respectively, into analog form. The analog waveforms produced by D/A converters 270 and 272 are provided with a local oscillator (LO) carrier frequency 10 signals $\text{Cos}(2\pi ft)$ and $\text{Sin}(2\pi ft)$, respectively, to mixers 288 and 290 where they are mixed and provided to summer 292. The quadrature phase carrier signals $\text{Sin}(2\pi ft)$ and $\text{Cos}(2\pi ft)$ are provided from suitable frequency sources (not shown). These mixed IF signals are summed in summer 292 and provided to mixer 294.

15 Mixer 294 mixes the summed signal with an RF frequency from frequency synthesizer 296 so as to provide frequency upconversion to the RF frequency band. The RF may then be bandpass filtered 298 and provided to an efficient parallel stage RF amplifier 10 of the invention. The filter 298 removes undesired spurs caused from upconversion 296. 20 Another filter (not shown) may be located following the amplifier circuitry to remove undesired spurs when the circuit is operating in bypass mode. In a bypass mode, the previous driver amplifier becomes the output amplifier and filtering may be necessary to prevent extra spurs 25 accomplished by another filter (not shown), thus the band-pass filter 298 may be located in the amplification path as illustrated in FIGS. 5, 6 and 7 discussed below. This also increases flexibility in choosing gain steps.

FIG. 5 illustrates a second embodiment of the invention wherein the power loss after the power amplifier is minimized. A driver amplifier 280 produces an analog signal, which is switched by a first 30 switch 20 between an amplifier path 28 and a bypass path 30. In the

amplifier path 28, the signal is band-pass filtered 298 and amplified by a power amplifier 32. The amplified signal is split by a first hybrid circuit 60 to produce an in-phase signal and a quadrature signal ninety degrees out of phase. Either of the in-phase signal or quadrature signal is 5 inverted by a coupler or a second hybrid circuit 64 to produce an inverted signal according to means known by those of ordinary skill in the art. The inverted signal and the un-inverted signal, i.e. the other of the in-phase or quadrature signal, are summed by a summing feature of the second hybrid circuit 64 and transmitted toward the RF-output port 54 10 or antenna (not shown). Prior to being transmitted from an antenna, the signal is again filtered by a filter (not shown) to reduce any unwanted spurs or other effects.

When the first switch 20 routes the signal to the bypass path 30, the signal is transmitted to an isolated port of the second hybrid circuit 64. 15 The second hybrid circuit 64 splits the signal into an in-phase signal and a quadrature signal ninety degrees out of phase. The first hybrid circuit 60 inverts either the in-phase signal or the quadrature signal and sums the two signals. The summed signal is transmitted to the output of the power amplifier 32. The power amplifier 32 in this scenario is turned off 20 to conserve power.

The turned-off power amplifier appears as a large impedance or a reflective load to the signal, which therefore reflects back to the first hybrid circuit 60. The reflected signal is split by the first hybrid circuit 60 into an in-phase signal and a quadrature signal ninety degrees out of 25 phase, input into the second hybrid circuit 64, where one of either the in-phase or quadrature signal is inverted. The inverted signal is summed with the other un-inverted signal, filtered, and transmitted to the output port 54 or antenna.

When the bypass path is used, a second switch 43 positioned in the 30 bypass path selectively connects the isolated port of the second hybrid circuit 64 with the first switch 20. However, when the amplifier path 28 is utilized, the second switch 43 selectively connects the isolated port of

the second hybrid circuit 64 to route reflected signals to a terminating resistor 45. When the power amplifier 32 is bypassed, the signal reflected off of the power amplifier 32 acting as a reflecting load is filtered by a filter (not shown) prior to being radiated by the antenna (not shown). The 5 circuit of the present invention does not need an output switch after the power amplifier, which simplifies the circuit and reduces the power loss after the power amplifier 32.

FIG. 6 illustrates a third and preferred embodiment of the present invention which provides greater minimization of power loss after the 10 amplifying the signal with power amplifiers. This embodiment provides a driver amplifier 280 producing an analog signal. The analog signal is switched by a first switch 20 between an amplifier path 28 and a bypass path 30. In the amplifier path, the signal is band-pass filtered 298, split by a first hybrid circuit 60 into an in-phase signal and a quadrature signal 15 ninety degrees out of phase. The in-phase signal and the quadrature signal are each independently amplified by a first amplifier 31 and a second amplifier 32, respectively. One of the amplified in-phase signal or the amplified quadrature signal is inverted by the second hybrid circuit 64 to produce an inverted signal. The inverted signal and the other un-inverted signal are summed in the second hybrid circuit 64, filtered by a 20 filter (not shown) and fed toward the RF-output port 54 or antenna (not shown).

The bypass path 30 provides a path from the first switch 20 to an isolated port of the second hybrid circuit 64. The signal is split into an in-phase signal and a quadrature signal the hybrid circuit 64. The in-phase signal is transmitted to the output of the first power amplifier 31 which is turned off and therefore appears as a reflective load to the signal. The quadrature signal is transmitted to the output of the second power amplifier 32, which is turned off and therefore appears as a reflective load 25 to the signal. Each reflected signal again enters the second hybrid circuit 64, where either the in-phase signal or the quadrature signal one of the split signals is inverted and summed with the other signal. The summed 30

signal is output to the output port 54. Each circuit in FIGS. 5 and 6 also contains a filter (not shown) after the power amplifier or power amplifiers. Accordingly, a signal reflected from the high impedance output of the power amplifier is still band-pass filtered to reduce 5 unwanted effects.

When the bypass path is used, a second switch 43 connects the isolated port of the hybrid circuit 64 with the first switch 20. However, when the amplifier path 28 is utilized, the switch 43 connects the isolated port of the second hybrid circuit 64 with ground through a resistor 45, 10 which routes any reflected signal to ground. The circuit of this arrangement does not need an output switch and therefore simplifies the circuit and reduces the power consumption.

Shunt switches 47a, 47b can be used to shunt the output of the power amplifiers 31, 32 when using the bypass path 30. This will ensure 15 that the output of each power amplifier 31, 32 is reflective without introducing significant loss. The shunt switches 47a, 47b could be implemented with a pin diode, FET switch or other means.

FIG. 7 is a fourth embodiment of the present invention wherein 20 the analog signal is switched by a first switch 20 between a bypass path 30 and an amplifier path 28. However, band-pass filtering 298 only occurs in the amplifier path 28. Accordingly, the signal is band-pass filtered 298 and fed to the power amplifier 32, amplified, and transmitted to the circulator 55, which routes the signal towards the RF-output port. When 25 the first switch 20 directs the analog signal through the amplifier path, the circulator 55 is connected to ground through a second switch 43 and a resistor 45. Accordingly, with this configuration, when reflected or returned RF-signals enter the circulator 55 from the direction of the RF-output port, the reflected signal is routed by the circulator 55 to ground. When the first switch 20 switches the analog signal to the bypass path 30, 30 the second switch 43 connects the bypass path 30 to the circulator 55, and the signal is routed toward the output of the amplifier. This will appear

as a high impedance, reflecting the signal back through isolator (shunt) 55 and to RF-output port 54.

As in FIG. 6, a shunt switch 47a may be used to shunt the output of power amplifier 32 when using the bypass path 30. This ensures that the 5 output of PA 32 is reflective without introducing significant loss. The shunt 47a may be a PIN diode, FET switch or other means.

FIG. 8 illustrates another aspect of the power amplifier circuit of FIG. 2 without the attenuating path 34. An analog signal is fed from a driver amplifier 280 through a band-pass filter 298 to a first switch 20.

10 The switch 20 alternates between a bypass path 30 and an amplifier path 28, wherein a power amplifier 32 amplifies the signal. A second switch 42 transmits the analog signal from either the bypass path 30 or the amplifier path 28 to a circulator 55, which routes the signal to the RF-output port 54.

15 The previous description of the preferred embodiment are provided to enable any person skilled in the art to make or use the present invention. Various modifications to those embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without the use of 20 the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown herein, but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

WE CLAIM:

CLAIMS

1. A power amplifier circuit arrangement, comprising:
 - 2 a driver amplifier for transmitting an analog signal;
 - 4 a first switch for selectively switching the analog signal between a bypass path and an amplifier path, said amplifier path comprising:
 - 6 a band-pass filter for filtering the analog signal and for producing a filtered signal;
 - 8 a power amplifier for receiving the filtered signal and for producing an amplified signal;
 - 10 a first hybrid circuit for splitting the amplified signal into an in-phase signal and a quadrature signal; and
 - 12 a second hybrid circuit for inverting the in-phase signal to produce an inverted signal and for summing the inverted signal and the quadrature signal to produce a summed signal,
 - 16 said bypass path connecting an output of said driver amplifier with an isolated port of said second hybrid circuit when said first switch switches the analog signal to said bypass path, whereby the analog signal transmitted from said driver amplifier will reflect off of said power amplifier and be routed to an output port.
2. The circuit arrangement of claim 1, further comprising:
 - 2 a second switch positioned in said bypass path; and
 - 4 a terminating resistor connected to a pole of said second switch,
 - 6 said second switch selectively connecting the isolated port of said second hybrid circuit with either said first switch or said terminating resistor.

3. The circuit arrangement of claim 1, wherein the analog
2 signal is a radio-frequency analog signal.

4. The power amplifier circuit arrangement of claim 1,
2 wherein said first switch switches the analog signal to said
bypass path when said power amplifier is turned off.

5. A power amplifier circuit arrangement, comprising:
2 a driver amplifier for transmitting an analog signal;
4 a first switch for selectively switching the analog signal
between a bypass path and an amplifier path, said amplifier path
comprising:
6 a band-pass filter for filtering the analog signal and
for producing a filtered signal;
8 a power amplifier for receiving the filtered signal
and for producing an amplified signal;
10 a first hybrid circuit for splitting the amplified signal
into an in-phase signal and a quadrature signal; and
12 a second hybrid circuit for inverting the quadrature
signal to produce an inverted signal and for summing the
14 inverted signal and the in-phase signal to produce a summed
signal,
16 said bypass path connecting an output of said driver
amplifier with an isolated port of said second hybrid circuit when
18 said first switch switches the analog signal to said bypass path,
whereby the analog signal transmitted from said driver amplifier
20 will reflect off of said power amplifier and be routed to an output
port.

6. The circuit arrangement of claim 5, further comprising:
2 a second switch positioned in said bypass path; and

a terminating resistor connected to a pole of said second
4 switch,

said second switch selectively connecting the isolated port
6 of said second hybrid circuit with either said first switch or said
terminating resistor.

7. The circuit arrangement of claim 5, wherein the analog
2 signal is a radio-frequency analog signal.

8. The power amplifier circuit arrangement of claim 5,
2 wherein said first switch switches the analog signal to said
bypass path when said power amplifier is turned off.

9. A method for amplifying a signal in a circuit having a
2 driver amplifier, an amplifier path comprising a first switch, a
band-pass filter, a power amplifier, a first hybrid circuit and a
4 second hybrid circuit, and a bypass path connecting an isolated
port of the second hybrid circuit to the first switch, said method
6 comprising:

(A) producing a driver signal from the driver amplifier;
8 (B) selectively switching the driver signal between the
amplifier path and the bypass path using the first switch,

10 wherein when the driver signal is switched in said
switching step to the amplifier path, said method further
12 comprises the steps of:

14 (a) band-pass filtering the driver signal by the
band-pass filter to produce a filtered signal;

16 (b) amplifying the filtered signal by the power
amplifier to produce an amplified signal;

18 (c) splitting the amplified signal into an in-phase
signal and a quadrature signal in the first hybrid circuit;

(d) inverting the in-phase signal to produce an
20 inverted signal in the second hybrid circuit; and

22 (e) summing the inverted signal and the
quadrature signal to produce a summed signal in the second
hybrid circuit,

24 and wherein when the driver signal is switched in said
switching step to the bypass path, said method further comprises
26 the steps of:

28 (a) turning off the power amplifier;
30 (b) transmitting the driver signal to the isolated
port of the second hybrid circuit;
(c) reflecting the driver signal off an output of
the power amplifier to an output port.

10. The method of claim 9, wherein the circuit further
2 comprises a second switch positioned in the bypass path, said
method further comprising:

4 selectively switching the second switch between connecting
the isolated port of the second hybrid circuit to a terminating
6 resistor and connecting the isolated port of the second hybrid
circuit to the first switch.

11. The method for amplifying a signal of claim 9, wherein the
2 driver signal is a radio-frequency analog signal.

12. A method for amplifying a signal in a circuit having a
2 driver amplifier, an amplifier path comprising a first switch, a
band-pass filter, a power amplifier, a first hybrid circuit and a
4 second hybrid circuit, and a bypass path connecting an isolated
port of the second hybrid circuit to the first switch, said method
6 comprising:

(A) producing a driver signal from the driver amplifier;

8 (B) selectively switching the driver signal between the
amplifier path and the bypass path using the first switch,
10 wherein when the driver signal is switched in said
switching step to the amplifier path, said method further
12 comprises the steps of:

(a) band-pass filtering the driver signal by the
14 band-pass filter to produce a filtered signal;

16 (b) amplifying the filtered signal by the power amplifier to produce an amplified signal;

(c) splitting the amplified signal into an in-phase signal and a quadrature signal in the first hybrid circuit;

20 (d) inverting the in-phase signal to produce an inverted signal in the second hybrid circuit; and

22 (e) summing the inverted signal and the quadrature signal to produce a summed signal in the second hybrid circuit,

24 and wherein when the driver signal is switched in said
switching step to the bypass path, said method further comprises
26 the steps of:

(a) turning off the power amplifier;

28 (b) transmitting the driver signal to the isolated port of the second hybrid circuit;

30 (c) reflecting the driver signal off an output of the power amplifier to an output port.

13. The method of claim 12, wherein the circuit further
2 comprises a second switch positioned in the bypass path, said
method further comprising:

4 selectively switching the second switch between connecting
the isolated port of the second hybrid circuit to a terminating
6 resistor and connecting the isolated port of the second hybrid
circuit to the first switch.

14. The method for amplifying a signal of claim 12, wherein
2 the driver signal is a radio-frequency analog signal.

15. A power amplifier circuit arrangement, comprising:
2 a driver amplifier for transmitting an analog signal;
4 a first switch for switching the analog signal between a
bypass path and an amplifier path, said amplifier path
comprising:
6 a band pass filter which filters the analog signal to
produce a filtered signal;
8 a first hybrid circuit for splitting the filtered signal
into an in-phase signal and a quadrature signal;
10 a first power amplifier for amplifying the in-phase
signal to produce a first amplified signal;
12 a second power amplifier for amplifying the
quadrature signal to produce a second amplified signal; and
14 a second hybrid circuit for inverting the first
amplified signal to produce an inverted signal and for summing
16 the inverted signal and the second amplified signal,
said bypass path connecting an output of said driver
18 amplifier and an isolated port of said second hybrid circuit when
said first switch switches the analog signal to said bypass path.

16. A power amplifier circuit arrangement, comprising:
2 a driver amplifier for transmitting an analog signal;
4 a first switch for switching the analog signal between a
bypass path and an amplifier path, said amplifier path
comprising:
6 a band pass filter which filters the analog signal to
produce a filtered signal;

8 a first hybrid circuit for splitting the filtered signal
into an in-phase signal and a quadrature signal;
10 a first power amplifier for amplifying the in-phase
signal to produce a first amplified signal;
12 a second power amplifier for amplifying the
quadrature signal to produce a second amplified signal; and
14 a second hybrid circuit for inverting the second
amplified signal to produce an inverted signal and for summing
16 the inverted signal and the first amplified signal,
 said bypass path connecting an output of said driver
18 amplifier and an isolated port of said second hybrid circuit when
said first switch switches the analog signal to said bypass path.

17. The power amplifier circuit arrangement of claim 15,
2 wherein the analog signal is a radio-frequency analog signal.

18. The power amplifier circuit arrangement of claim 16,
2 wherein the analog signal is a radio-frequency analog signal.

19. The power amplifier circuit arrangement of claim 15,
2 wherein said switch switches to said bypass path when the power
amplifier is turned off.

20. The power amplifier circuit arrangement of claim 16,
2 wherein said switch switches to said bypass path when the power
amplifier is turned off.

21. The circuit arrangement of claim 15 further comprising:
2 a second switch positioned in said bypass path; and
 a terminating resistor connected to a pole of said second
4 switch,

6 said second switch selectively connecting the isolated port
6 of said second hybrid circuit with either said first switch or said
terminating resistor.

22. The circuit arrangement of claim 16 further comprising:
2 a second switch positioned in said bypass path; and
4 a terminating resistor connected to a pole of said second
4 switch,

6 said second switch selectively connecting the isolated port
6 of said second hybrid circuit with either said first switch or said
terminating resistor.

23. The circuit arrangement of claim 15 further comprising:
2 a first shunt switch positioned between said first power
amplifier and said second hybrid circuit; and
4 a second shunt switch positioned between said second
power amplifier and said second hybrid circuit;
6 said first and second shunt switches being used to shunt
the output of said first and second power amplifiers, respectively,
8 when using said bypass path.

24. The circuit arrangement of claim 16 further comprising:
2 a first shunt switch positioned between said first power
amplifier and said second hybrid circuit; and
4 a second shunt switch positioned between said second
power amplifier and said second hybrid circuit;
6 said first and second shunt switches being used to shunt
the output of said first and second power amplifiers, respectively,
8 when using said bypass path.

25. A method for amplifying a signal in a circuit having a
2 driver amplifier, an amplifier path comprising a first switch, a

band-pass filter, a first power amplifier, a second power amplifier,
4 a first hybrid circuit and a second hybrid circuit, and a bypass path
connecting an isolated port of the second hybrid circuit with the
6 first switch, said method comprising:

(A) producing a driver signal from the driver amplifier;
8 (B) selectively switching the driver signal between the
amplifier path and the bypass path using the first switch,

10 wherein when the driver signal is switched in said
switching step to the amplifier path, said method further
12 comprises:

(a) band-pass filtering the driver signal by the
14 band-pass filter to produce a filtered signal;

(b) splitting the filtered signal in the first hybrid
16 circuit into an in-phase signal and a quadrature signal;

(c) amplifying the in-phase signal by the first
18 power amplifier to produce an amplified in-phase signal;

(d) amplifying the quadrature signal by the
20 second power amplifier to produce an amplified quadrature
signal;

(e) inverting the amplified in-phase signal in the
22 second hybrid circuit to produce an inverted signal; and

(f) summing the inverted signal and the
24 amplified quadrature signal in the second hybrid circuit to
26 produce a summed signal,

and wherein when the driver signal is switched in said
28 switching step to the bypass path, said method further
comprises:

30 (a) turning off the first power amplifier and the
second power amplifier;

32 (b) transmitting the driver signal to the isolated
port of the second hybrid circuit;

34 (c) splitting the driver signal into an in-phase signal and a quadrature signal in the second hybrid circuit;

36 (d) reflecting the in-phase signal off of the first amplifier signal;

38 (e) reflecting the quadrature signal off of the second power amplifier;

40 (f) inverting the reflected in-phase signal in the second hybrid circuit to produce an inverted signal;

42 (g) summing the inverted signal and the quadrature signal in the second hybrid circuit to produce a

44 summed signal; and

46 (h) outputting the summed signal to an output port.

26. A method for amplifying a signal in a circuit having a
2 driver amplifier, an amplifier path comprising a first switch, a
4 band-pass filter, a first power amplifier, a second power amplifier,
6 a first hybrid circuit and a second hybrid circuit, and a bypass path
connecting an isolated port of the second hybrid circuit with the
first switch, said method comprising:
8 (A) producing a driver signal from the driver amplifier;
10 (B) selectively switching the driver signal between the
amplifier path and the bypass path using the first switch,
12 wherein when the driver signal is switched in said
switching step to the amplifier path, said method further
comprises:
14 (a) band-pass filtering the driver signal by the
band-pass filter to produce a filtered signal;
16 (b) splitting the filtered signal in the first hybrid
circuit into an in-phase signal and a quadrature signal;
18 (c) amplifying the in-phase signal by the first
power amplifier to produce an amplified in-phase signal;

20 (d) amplifying the quadrature signal by the
second power amplifier to produce an amplified quadrature
signal;

22 (e) inverting the amplified quadrature signal in
the second hybrid circuit to produce an inverted signal; and

24 (f) summing the inverted signal and the
amplified in-phase signal in the second hybrid circuit to produce
26 a summed signal,

28 and wherein when the driver signal is switched in said
switching step to the bypass path, said method further comprises:

30 (a) turning off the first power amplifier and the
second power amplifier;

32 (b) transmitting the driver signal to the isolated
port of the second hybrid circuit;

34 (c) splitting the driver signal into an in-phase
signal and a quadrature signal in the second hybrid circuit;

36 (d) reflecting the in-phase signal off of the first
amplifier signal;

38 (e) reflecting the quadrature signal off of the
second power amplifier;

40 (f) inverting the reflected quadrature signal in
the second hybrid circuit to produce an inverted signal;

42 (g) summing the inverted signal and the in-
phase in the second hybrid circuit to produce a summed signal;
and

44 (h) outputting the summed signal to an output
port.

27. The method for amplifying a signal of claim 25 wherein
2 the driver signal is a radio-frequency analog signal.

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28. The method for amplifying a signal of claim 26 wherein
2 the driver signal is a radio-frequency analog signal.

29. The method of claim 25 wherein the circuit further
2 comprises a second switch positioned in the bypass path, said
method further comprising:

4 selectively switching the second switch between connecting
the isolated port of the second hybrid circuit to a terminating
6 resistor and connecting the isolated port of the second hybrid
circuit to the first switch.

30. The method of claim 26 wherein the circuit further
2 comprises a second switch positioned in the bypass path, said
method further comprising:

4 selectively switching the second switch between connecting
the isolated port of the second hybrid circuit to a terminating
6 resistor and connecting the isolated port of the second hybrid
circuit to the first switch.

31. A mobile communication unit having a power supply, a
2 digital processor, a receiving chain, a transmitting chain, a
duplexer, an antenna, and user interfacing means, said mobile
4 communication unit comprising:

6 a power amplifier circuit arrangement in said transmitting
chain, said power amplifier circuit comprising:

8 a driver amplifier for transmitting an analog signal;

10 a first switch for selectively switching the analog signal
between a bypass path and an amplifier path, said amplifier path
comprising:

12 a band-pass filter for filtering the analog signal and
for producing a filtered signal;

14 a power amplifier for receiving the filtered signal
14 and for producing an amplified signal;
16 a first hybrid circuit for splitting the amplified signal
16 into an in-phase signal and a quadrature signal; and
18 a second hybrid circuit for inverting the in-phase
18 signal to produce an inverted signal and for summing the
18 inverted signal and the quadrature signal to produce a summed
20 signal,
22 said bypass path connecting an output of said driver
22 amplifier with an isolated port of said second hybrid circuit when
22 said first switch switches the analog signal to said bypass path,
24 whereby the analog signal transmitted from said driver amplifier
24 will reflect off of said power amplifier and be routed to an output
26 port.

32. The mobile communication unit of claim 31, wherein said
2 power amplifier circuit arrangement further comprises:
4 a second switch positioned in said bypass path; and
4 a terminating resistor connected to a pole of said second
4 switch,
6 said second switch selectively connecting the isolated port
6 of said second hybrid circuit with either said first switch or said
8 terminating resistor.

33. The mobile communication unit of claim 31, wherein said
2 first switch switches the analog signal to said bypass path when
2 said power amplifier is turned off.

34. A mobile communication unit having a power supply, a
2 digital processor, a receiving chain, a transmitting chain, a
2 duplexer, an antenna, and user interfacing means, said mobile
4 communication unit comprising:

6 a power amplifier circuit arrangement in said transmitting chain, said power amplifier circuit arrangement comprising:

8 a driver amplifier for transmitting an analog signal;

10 a first switch for switching the analog signal between a bypass path and an amplifier path, said amplifier path comprising:

12 a band pass filter which filters the analog signal to produce a filtered signal;

14 a first hybrid circuit for splitting the filtered signal into an in-phase signal and a quadrature signal;

16 a first power amplifier for amplifying the in-phase signal to produce a first amplified signal;

18 a second power amplifier for amplifying the quadrature signal to produce a second amplified signal; and

20 a second hybrid circuit for inverting the first amplified signal to produce an inverted signal and for summing 22 the inverted signal and the second amplified signal,

24 said bypass path connecting an output of said driver amplifier and an isolated port of said second hybrid circuit when said first switch switches the analog signal to said bypass path.

35. The mobile communication unit of claim 34, wherein said 2 power amplifier circuit arrangement further comprises:

4 a second switch positioned in said bypass path; and

6 a terminating resistor connected to a pole of said second switch;

8 said second switch selectively connecting the isolated port of said second hybrid circuit with either said first switch or said terminating resistor.

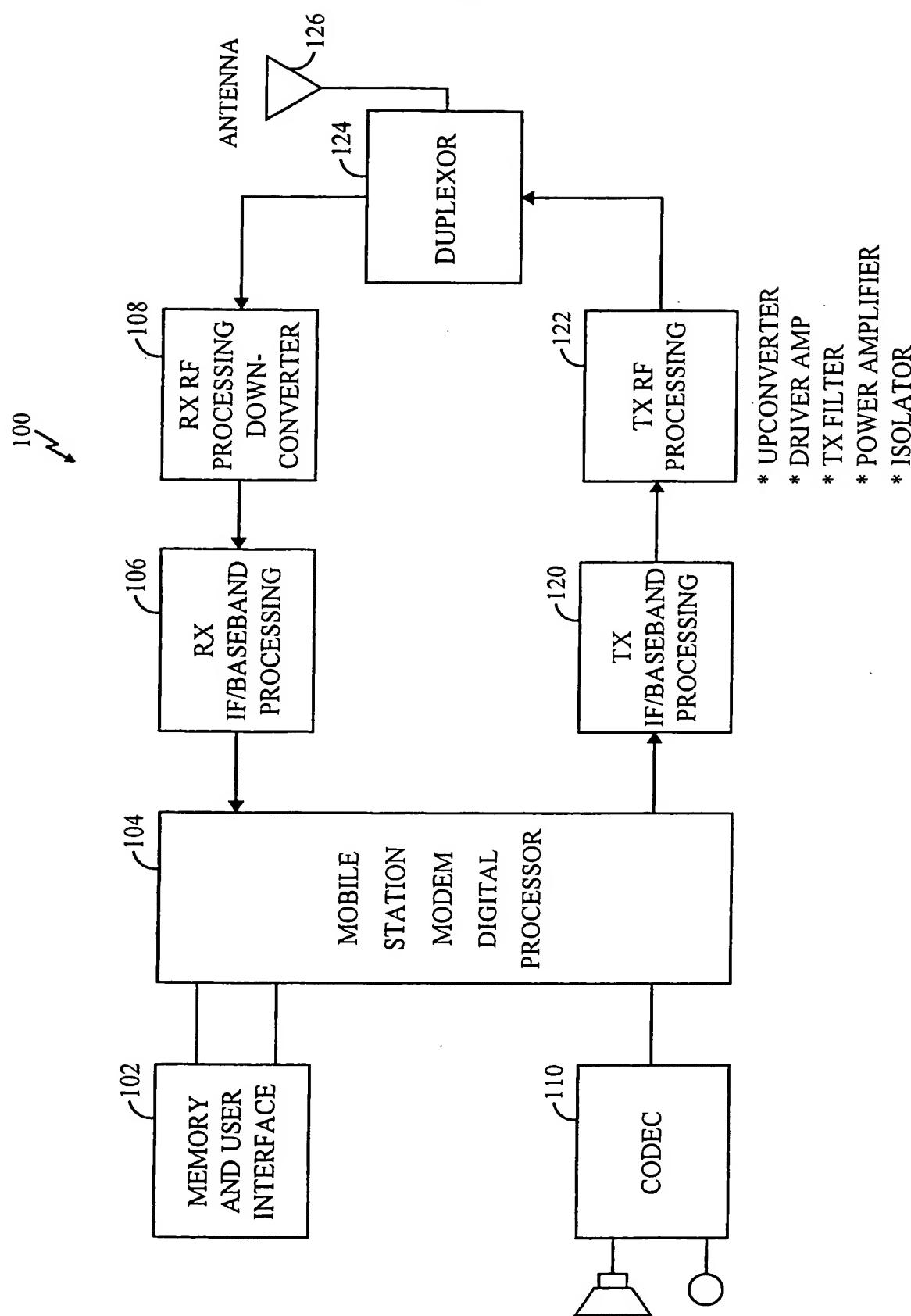


FIG. 1

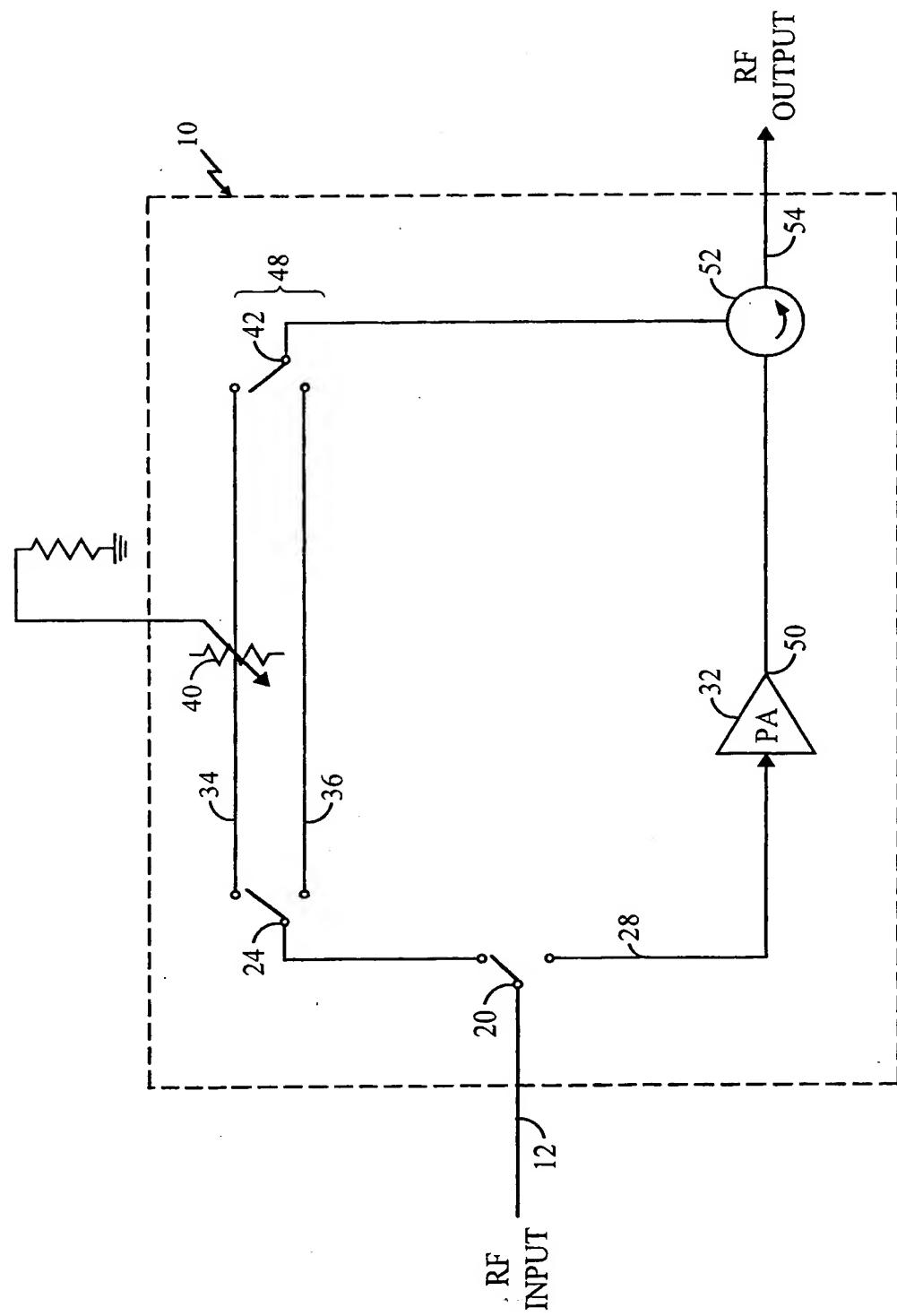


FIG. 2

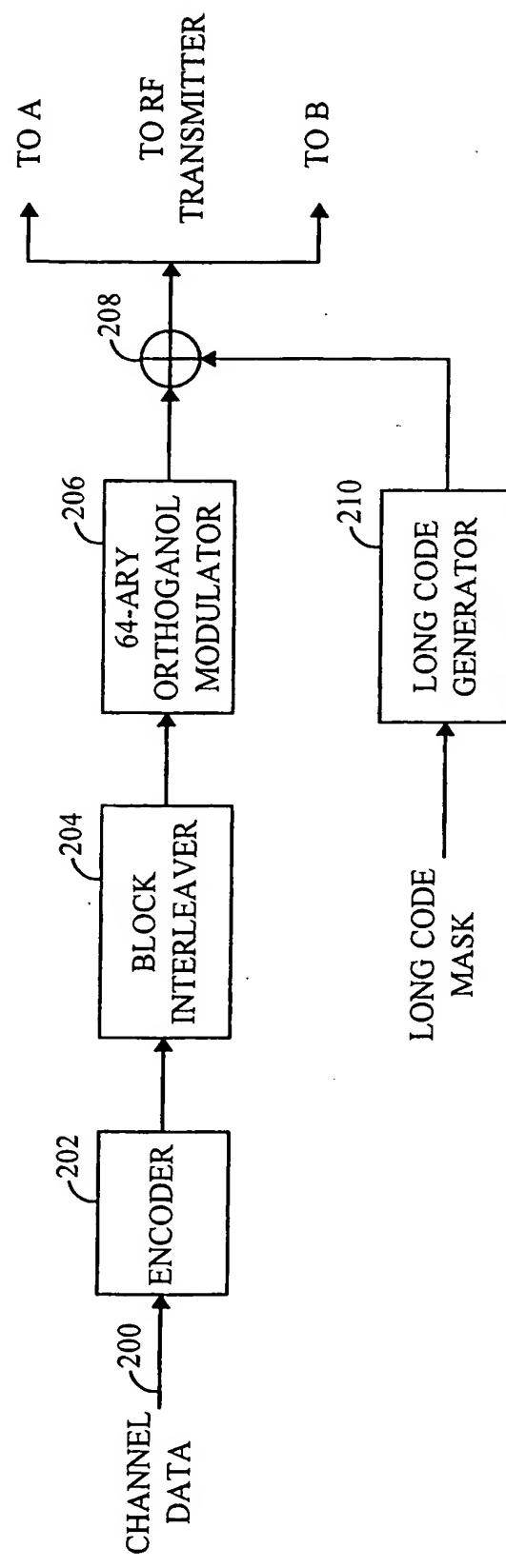


FIG. 3

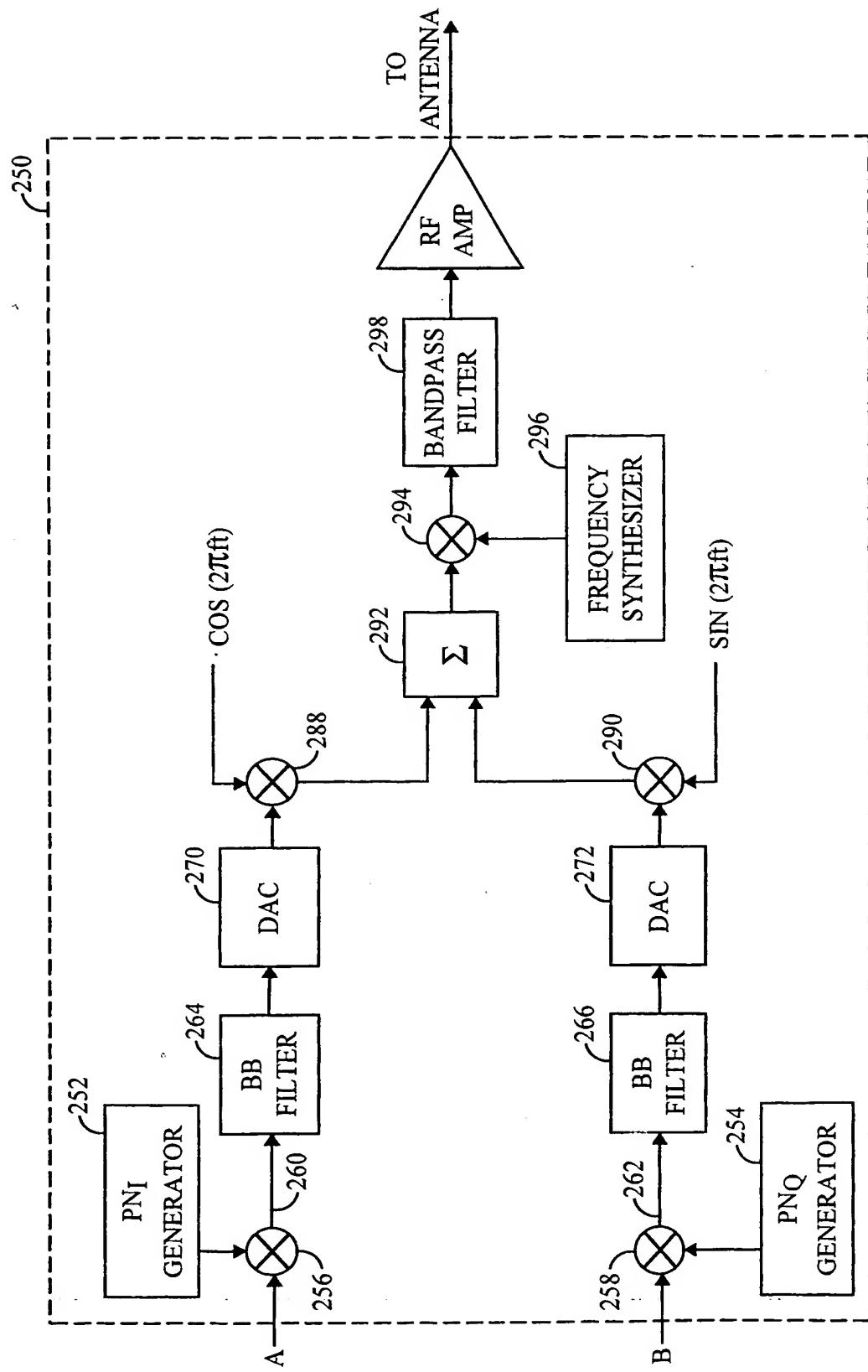


FIG. 4

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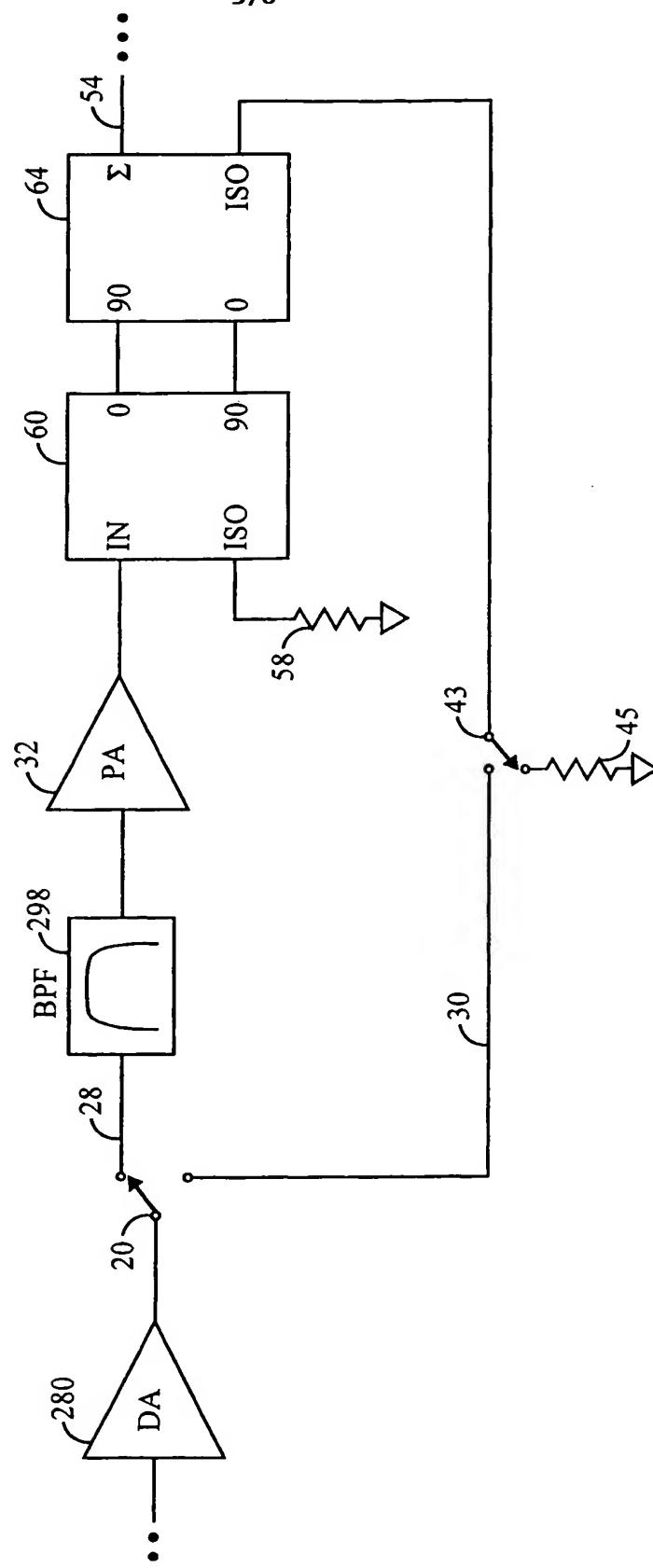


FIG. 5

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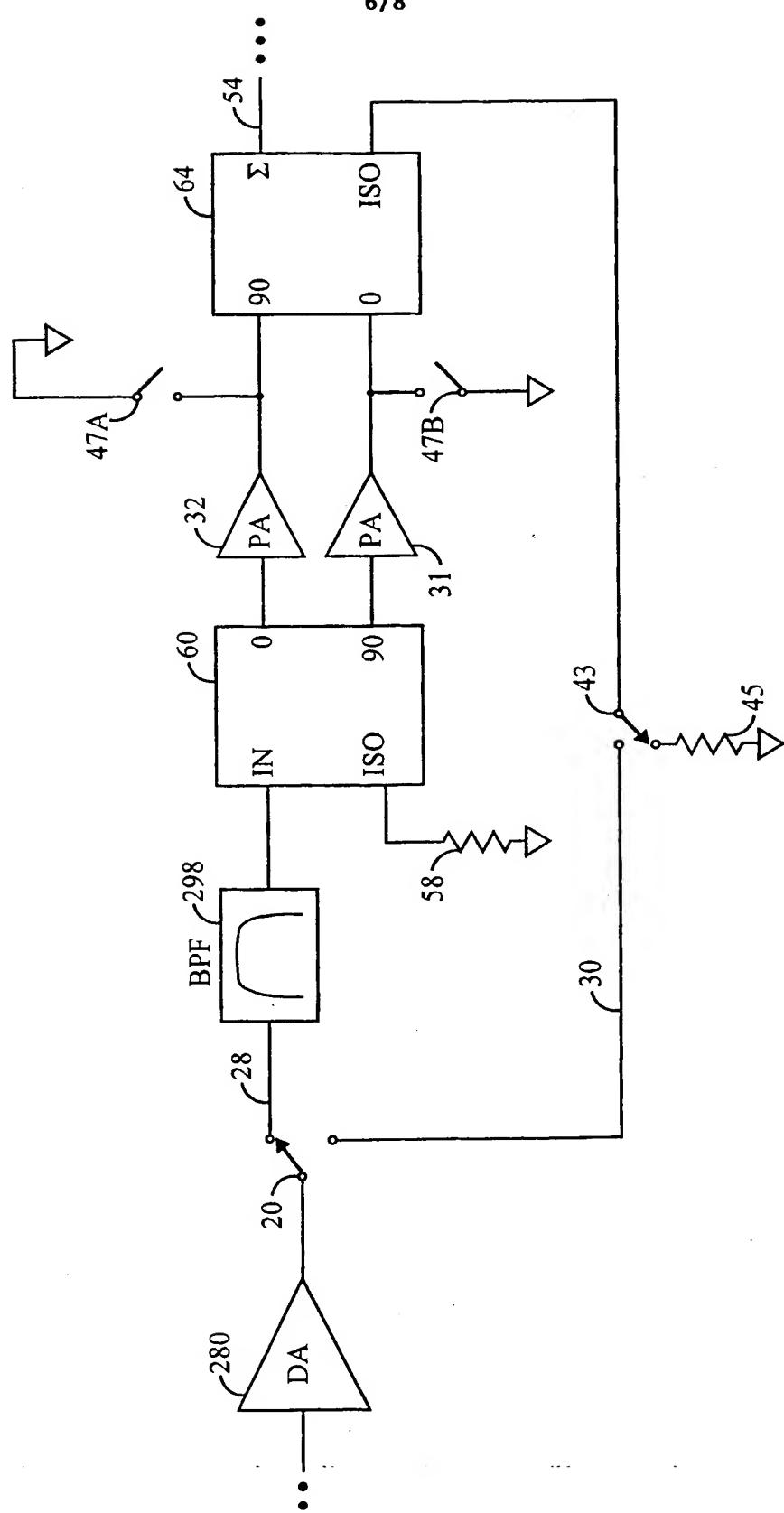


FIG. 6

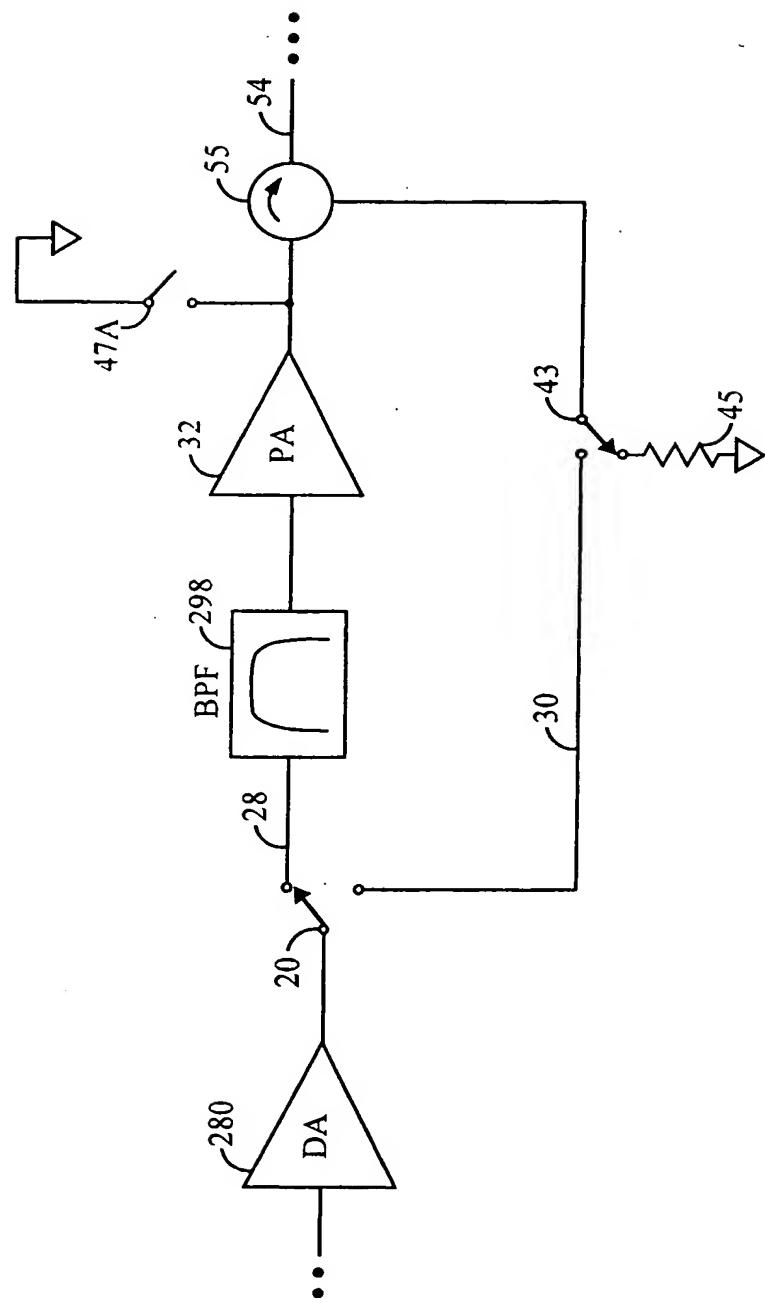


FIG. 7

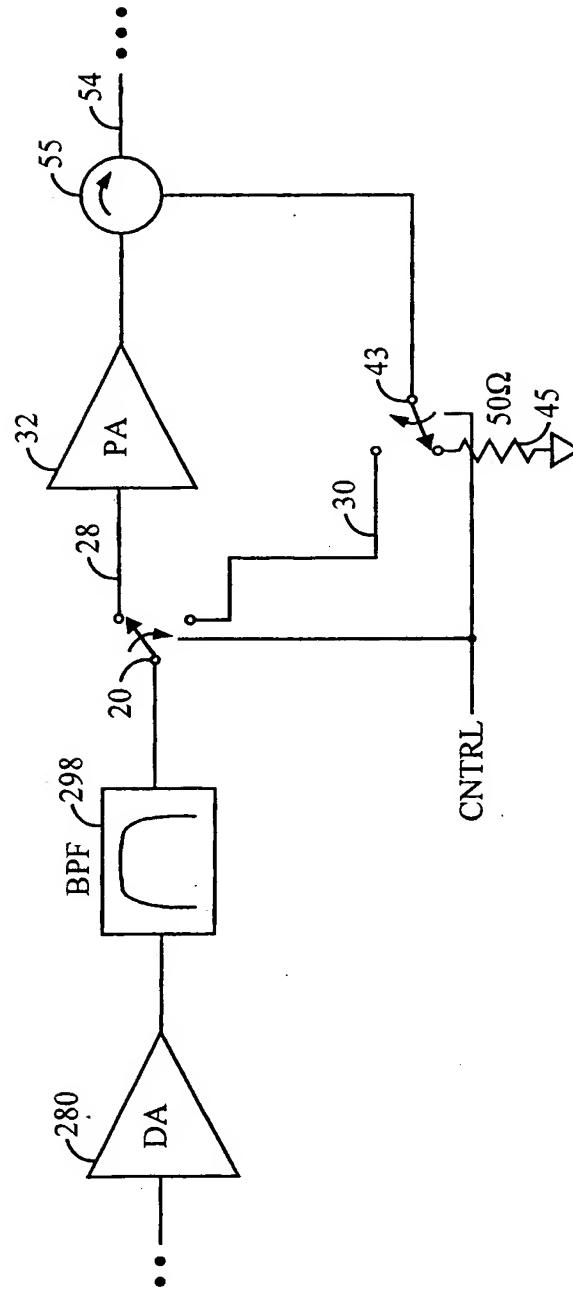


FIG. 8

INTERNATIONAL SEARCH REPORT

Internat'l Application No
PCT/US 99/21757A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/72 H03G1/00 H03F3/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F H03G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 093 667 A (ANDRICOS CONSTANTINE) 3 March 1992 (1992-03-03) column 8, line 32 -column 9, line 42; figures 6,7	1-30
A	WO 97 24800 A (QUALCOMM INC) 10 July 1997 (1997-07-10) page 17, line 36 -page 20, line 5; figure 8	1-35
A	US 4 010 426 A (RAMBO SHELDON I) 1 March 1977 (1977-03-01) column 2, line 6 - line 47; figure 1	1

 Further documents are listed in the continuation of box C. Patent family members are listed in annex.

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Date of the actual completion of the International search

20 December 1999

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Internat'l Application No

PCT/US 99/21757

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